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accessible from outside the board, via one and the same path from a specific terminal of the board, the transfer of the data sensed or to be imposed taking place in series in this path.

Through such arrangements, the Boundary Scan also permits the testing of the interconnections between the integrated circuits on a board. In this case, the test vector is loaded serially into the Boundary Scan path, then sent to the interconnections to be tested via output buffers of the components. The results are sampled in the Boundary Scan, via the inputs of the components, then output serially to the tester.

In an "internal test" mode, adapted for testing the components themselves, a test vector is loaded in

series in the Boundary Scan path and then applied to the internal logic of the integrated circuit. The result is sampled in the Boundary Scan path, then read serially by the tester.

This second test process has drawbacks: it is especially lengthy to implement, particularly in the internal mode where the components of the board are tested. Moreover, this test process turns out to be especially unsuitable for the testing of integrated circuits before they are mounted, in particular for testing integrated circuits which comprise memory elements.

US 5 850 513 also discloses a system allowing the checking of operational data of a circuit, including a maintenance subsystem, a flash memory, a controller, a processing unit, a main memory module, a data path network, means forming a dual bus, programmable logic control means, an auxiliary data transfer nozzle, and a series of input/output modules.

Together, these components process blocks of data of microcodes. The elements such as associated in this document, do not allow testing of the integrated circuit without multiple connections. This document does not therefore afford a satisfactory solution to the particularly lengthy implementation of customary testing processes.

The aim of the invention is to resolve these various drawbacks, by proposing a process for testing integrated circuits not requiring the connection of all the inputs/outputs of this circuit to a tester and making it possible to test an extended area, or even the entire circuit, it being possible moreover for this process to be carried out much faster than the known test processes.

Stated otherwise, the invention proposes to improve the coverage of an integrated circuit fabrication test as compared with the known full-scan ATPG method, without increasing the number of channels of the tester.

These aims are achieved according to the invention by virtue of a process for testing an integrated circuit comprising memory points and a Boundary Scan chain .

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